



Confirmation No.: 6199
Date of Notice of
Allowance: April 23, 2004
U.S. Serial No.: 09/997,589

UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Thomas J. Massingill, et al.
Confirmation No.: 6199
Serial No.: 09/997,589
Filed: November 29, 2001
For: *Multi-Chip Module and Method for Forming and Method for Deplating Defective Capacitors*
Art Group Unit: 1756
Examiner: Thai, Luan C.
Atty. Dkt.: 6136-53804 (25916-162)

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**CERTIFICATE OF
MAILING/TRANSMISSION
(37 C.F.R. § 1.8A)**

I hereby certify that this correspondence is,
on the date shown below, being:
 deposited with the United States Postal
Service with sufficient postage as first class
mail in an envelope addressed to:

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

transmitted by facsimile to the Patent and
Trademark Office.

7/23/04 
Date Jordan Wilson

Approved

2/24/05

L.T.

**LETTER TRANSMITTING FORMAL DRAWINGS
TO THE OFFICIAL DRAFTSPERSON.**

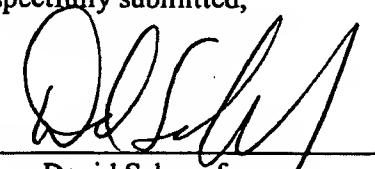
Sir:

Transmitted herewith are formal drawings for the above-identified application bearing Figures 1 – 87 on thirty-four (34) drawing sheets.

July 23, 2004
SHEPPARD MULLIN
Richter & Hampton LLP
Four Embarcadero Center, 17th Floor
San Francisco, CA 94111-4106
(415) 434-9100 (tel)
(415) 434-3947 (fax)

Respectfully submitted,

By


David Schnapf
Registration No. 31,566